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PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF THE RECORDING OF A CHANGE

(PCT Rule 92bis.1 and Administrative Instructions, Section 422)

To:

SCHÄFERJOHANN, Volker
Deutsche Thomson-Brandt GmbH
European Patent Operations
Karl-Wiechert-Allee 74
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ALLEMAGNE

Date of mailing (day/month/year) 27 August 2001 (27.08.01)	
Applicant's or agent's file reference PD990069	**IMPORTANT NOTIFICATION**
International application No. PCT/EP00/07395	**International filing date** (day/month/year) 31 July 2000 (31.07.00)

1. The following indications appeared on record concerning:

[X] the applicant [ ] the inventor [ ] the agent [ ] the common representative

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2. The International Bureau hereby notifies the applicant that the following change has been recorded concerning:

[X] the person [ ] the name [ ] the address [ ] the nationality [X] the residence

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3. Further observations, if necessary:

4. A copy of this notification has been sent to:

[X] the receiving Office
[ ] the International Searching Authority
[ ] the International Preliminary Examining Authority
[X] the designated Offices concerned
[ ] the elected Offices concerned
[ ] other:

The International Bureau of WIPO **34, chemin des Colombettes** **1211 Geneva 20, Switzerland**	Authorized officer R. Chrem
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Form PCT/IB/306 (March 1994) 004238724

PATENT COOPERATION TREATY

THOMSON multimedia
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Patent Department
Administration-Hannover

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From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:

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NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Rule 71.1)

Date of mailing *(day/month/year)*	03.01.2002
Applicant's or agent's file reference PD990069	**IMPORTANT NOTIFICATION**

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/EP00/07395	31/07/2000	30/09/1999

Applicant
DEUTSCHE THOMSON-BRANDT GMBH

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices) (Article 39(1)) (see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

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European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Thomas, R Tel.+49 89 2399-2247

Form PCT/IPEA/416 (July 1992)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

12

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
PD990069		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/EP00/07395	31/07/2000	30/09/1999
International Patent Classification (IPC) or national classification and IPC G09G3/28		
Applicant DEUTSCHE THOMSON-BRANDT GMBH		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 9 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 3 sheets.

3. This report contains indications relating to the following items:

I	☒	Basis of the report
II	☐	Priority
III	☐	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
IV	☐	Lack of unity of invention
V	☒	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
VI	☐	Certain documents cited
VII	☒	Certain defects in the international application
VIII	☒	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
19/04/2001	03.01.2002
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Morris, D Telephone No. +49 89 2399 2182

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/EP00/07395

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:
Description, pages:

1-15 as originally filed

Claims, No.:

1-8 as received on 25/10/2001 with letter of 25/10/2001

Drawings, sheets:

1/5-5/5 as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language: , which is:

- ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
- ☐ the language of publication of the international application (under Rule 48.3(b)).
- ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- ☐ contained in the international application in written form.
- ☐ filed together with the international application in computer readable form.
- ☐ furnished subsequently to this Authority in written form.
- ☐ furnished subsequently to this Authority in computer readable form.
- ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
- ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:

☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

(Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-8
	No:	Claims	
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-8
Industrial applicability (IA)	Yes:	Claims	1-8
	No:	Claims	

2. Citations and explanations
see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:
see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:
see separate sheet

Re Item V

Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1.1 Reference is made to the following documents

D1: EP 0888004 A (PIONEER ELECTRONIC CORP) 30 December 1998 (1998-12-30)

D2: EP 0924683 A (GRUNDIG) 23 June 1999 (1999-06-23)

D3: WO 9930309 A (MATSUSHITA) 17 June 1999 (1999-06-17)

D4: JP 6259034 A (FUJITSU GENERAL LTD) 16 September 1994 (1994-09-16)

D5: EP 1026655 A (DEUTSCHE THOMSON-BRANDT)

1.2 The documents D3 and D4 were not cited in the international search report. Copies of the documents are appended hereto.

1.3 The document D5 is the publication based on the European Patent Application EP 99101977.9 cited by the applicant in the disclosure (- cf. e.g. page 14, line 23 of the present application)

2.1 D1 discloses (- cf. independent claim 1):

a method for power level control (- "controlling brightness of a video signal" - column 1, lines 8-9) in a display device (- "plasma display panel" - Fig. 1 and column 6, line 47; - **cf.** claim 8) having a plurality of display elements corresponding to the pixels of a picture, wherein a power level mode selection process is used for increasing the peak white enhancement factor (- multipliers 110-112 - Fig. 3) of the display, said method comprising the steps of:

[measuring] the power level of a video picture (- APL calculating circuit 105 - Fig. 3 and column 9, lines 42-57);

[selecting] a corresponding power level mode for controlling the display contrast (- coefficient setting circuit 109 - Fig. 3 and column 10, lines 15-22); and

[dividing] the picture into a number of blocks (- " 8 blocks, which is obtained by dividing the video signal of one picture plane by 8 in a vertical

direction of the picture plane" - column 9, lines 48-50);

[summing up, in each block,] the video signals or values derived from the video signals of the colour components of the pixels in order to determine the local power values (- "synthesised into one brightness level" - column 9, lines 43-44 and "104" - Fig. 3) for the picture;

and

[performing] a local temperature estimation [for each block] based on said local power values (- see "APL calculating 105" - Fig. 3, "added values" - column 10, lines 3-14, and "heating or calorific value" of column 11, lines 25-29, i.e. it being noted that both the "average power" of determined by the APL 105 for a block and the heat generated by a plasma display element of said block are proportional to current flow required by the plasma element).

2.1a It is acknowledged that D1 fails to disclose the step of (- see wording of last four lines of present independent claim 1):

[selecting] a maximum local temperature in the display;

[determining] a maximum power level limit based on the determined maximum local temperature; and

[using] the power level limit to restrict the range of selectable power level modes in the power level mode selection process to power level modes having a power level below or equal to said power limit.

2.2 However D3, which also discloses corresponding features of:

power level control (- Brightness Detector 26, 28 together with Image Characteristics Determining Device 30 - Fig. 11);

a display device (- PDP - Fig. 11); and

a power level mode selection process (- see Tables 1-6 of pages 12-14; - cf. also "power level modes of EP 9910977.9 [- i.e. D5]" of page 14, line 23 together with "different power level modes for peak white enhancement" of Fig. 2 of D5).

2.2a Furthermore, D3 also discloses (- cf. lines 7-10 of present independent claim 1) a method of power level control comprising steps of:

[measuring] the power value of a video picture (- "Average Level Detector

28" and "L_{av}" - Fig. 11); and

[selecting] a corresponding power level for controlling the display contrast (- i.e. selecting one of 1-times mode to 6-times mode in accordance with "L_{av}" - Fig. 12).

2.2b In addition, insofar as D3 also discloses:

- determining and selecting the peak power level of a video picture (- Peak Level detector 26 and "Lpk" - Fig. 11); and
- using the peak power level to restrict the number of "Times" modes which can be used (- i.e. when "Lpk" is close to 100%, all "Times" modes 1-6 can be used, and when Lpk is close to 0%, only "1-Times" mode can be used - Fig. 12), said restricted number of power level modes by implicit definition having average power levels below or equal to the determined peak power level,

D3 is also considered to disclose respective steps of:

- selecting;
- determining; and
- using

of lines 15-27 of present independent claim 1 of the most recently received amended claims.

2.3 As such therefore, it appears the subject matter claimed in respect of present independent claim 1 is distinguished from that of the disclosure of D3 merely by the feature of the "picture divided [into] a number of blocks" of lines 11-15 of present independent claim 1.

2.4 However, as acknowledged in D1, it is well known in the art to:

- divide a picture plane into a plurality of blocks (- see "plurality of blocks" - column 2, lines 1-2 of D1);
- select a peak average from the respective averages of a plurality of blocks (- see "when an APL [..] in just one block exceeds a value" - column 2, lines 4-6 of D1); and
- obtain an average value for the average level of the picture (- "it is also possible to compare an averaged value of the added values [for each block] with the reference value" - column 11, lines 38-39).

Subsequently it appears that the subject matter of present independent claim 1 comprises no more than:

- the use of the teaching of D1 (- i.e. using "blocks" for determining peak or average values in the display of video pictures on a PDP)
- within a display in accordance with the teaching of D3 (- i.e. D3 disclosing a PDP using a combination of determined peak and average power levels for use in selecting driving modes),

whereupon the subject matter is considered to comprise no more than the use of a well known equivalent in a known display device.

Accordingly, so far as understood and in light of PCT Guidelines IV-Annex, 1.1(ii), the respective subject matters of independent claim 1 is not considered to involve an inventive step (- Article 33(3) PCT) over a non-inventive combination of the teachings of D1 and D3.

2.5 In addition, insofar the respective apparatus of present claims 7 and 8 appear to merely comprise corresponding means and/or circuits for implementing the steps in present independent claim 1, the respective subject matters of the apparatus of present independent claim 7, and dependent claim 8, are likewise not considered to involve an inventive step (- Article 33(3) PCT) over a non-inventive combination of the teachings of D1 and D3.

2.6 Furthermore, insofar as D1 discloses:

> "Two APLs in two blocks adjacent to each other, which have been calculated by the APL calculating circuit 105 in this manner, are added to each other by the APL adding circuit 106. F" - column 10, lines 3-6,

D1 is also considered to disclose (- cf. dependent claim 2):

- the power dissipation [..] of a number of neighbouring blocks is taken into account.

Accordingly, so far as understood, the subject matter of dependent claim 2 is also not considered to involve an inventive step (- Article 33(3) PCT) over a non-inventive combination of the teachings of D1 and D3.

2.7 Dependent claims 3-5 appear to relate to no more than routine measures well known to the skilled person for which no special effect or unexpected improvement appears to be achieved, and in respect of which the subject matter of said claims cannot be considered to comprise an inventive step over D1 within the meaning of Article 33(3) PCT.

2.8 The subject matter of dependent claim 6 appears directed subject matter of a method wherein a delay between power level modes is used, i.e. in accordance with whether the average power level of the video picture on the display is rising and falling, in order to prevent oscillation between power level modes under circumstances in which small changes in average power level occur.

However, the teaching of using such a delay in order to overcome said problem of oscillation in respect of switching power levels of a PDP is considered to be well known in the art, as indicated in D4 (- see PDP 15 - Fig. 6(a) of D4 and respective (l)ow, (h)igh, and (m)iddle lines of APL curves 1-3 of Fig. 6(b)). The subject matter of dependent claim 6 is therefore considered to comprise no more than a matter of routine, providing no surprising effect or unexpected benefit over that already known by the person skilled in the art.

Accordingly, the subject matter of dependent claim 6 is also not considered to involve an inventive step over a non-inventive combination of the teachings of D1 and D3 within the meaning of Article 33(3) PCT.

Re Item VII

Certain defects in the international application

3.1 D3 does not form the preamble of any Independent claim (Rule 6.3(b)(i) PCT).

3.2 Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the documents D1-D4 are not mentioned in the description, nor are these documents identified therein.

Re Item VIII

Certain observations on the international application

4. The following objections are made with respect to clarity (- Article 6 PCT) and disclosure (- Article 5 PCT).

4.1 The term "to restrict the range of selectable power level modes" of present independent claim 1 is considered obscure as the wording of the claim fails to explicitly define in what respect:

- increases of a Peak White Enhancement Factor (PWEF) of the display (- cf. lines 3-4 of amended independent claim 1) may be affected by said restriction of "power level modes"; or
- how a "power level" of a "power level mode" may be determined for purposes of comparison with levels of other "power level modes".

Subsequently the subject matter of present independent claim 1 appears to lack features considered essential for the performance and definition of the invention. As such therefore , in light of PCT Guidelines III-4.3 and 4.4, the subject matter of independent claim 1 is not considered to meet the requirements of Article 6 PCT.

4.2 Insofar as the example given in description of:

- "then only the first 34 power level modes of EP 99101977.9 are selectable for PWEF control" (- page 14, lines 23-24 as originally filed),

appears to relate directly to the disclosure of the invention (- cf. also "to restrict the range of selectable power modes" of the wording of present amended claim 1), the matter of said underlined European Application relating to said "power level modes" should be incorporated in the description of the present application (- PCT Guidelines II-4.17; Article 5 PCT).

Claims

1. Method for power level control in a display device having a plurality of display elements corresponding to the pixels of a picture, wherein a power level mode selection process is used for increasing the peak white enhancement factor of the display, in which the power value of a video picture is measured and a corresponding power level mode is selected for controlling the display contrast, wherein a picture is divided in a number of blocks (S_{11}-S_{58}), wherein in each block (S_{11}-S_{58}) the video levels or values derived from the video levels of the colour components of the pixels are summed up in order to determine the local power values (LP) for the picture, **characterised in that** a local temperature estimation is performed for the corresponding blocks of the display based on said local power values (LP) and the previously estimated local temperature values, wherein in the estimated local temperature values the maximum local temperature (MT) in the display is selected, wherein a further step of maximum power level limit (PLM) determination is performed based on the maximum local temperature (MT), and wherein the power level limit (PLM) is used to restrict the range of selectable power level modes in the power level mode selection process to power level modes having a power level below or equal to said power level limit (PLM).

2. Method according to claim 1, wherein for local temperature estimation of a block (S_{11}-S_{58}), the power dissipation not only of the local block (S_{11}-S_{58}) but also of a number of neighbouring blocks (S_{11}-S_{58}) is taken into account.

3. Method according to claim 1 or 2, wherein the maximum local temperature determination for the display is performed once in a number of video frames.

4. Method according to claim 3, wherein the steps of local power value determination and local temperature estimation are performed only for one or more selected blocks of the whole picture within a frame period.

5. Method according to claim 3 or 4, wherein a picture is divided in 40 blocks and the maximum local temperature determination is performed once within 40 frame periods.

6. Method according to one of claims 1 to 5, wherein the switching between maximum allowed power level limits corresponding to the determined maximum local temperature is controlled with a power level mode against picture power curve that falls if the picture power is increasing and that rises if the picture power is decreasing, and with a delay between falling and rising, respectively rising and falling if the change direction of the picture power value changes.

7. Apparatus for carrying out the method according to one of the previous claims, the apparatus having included a power level determination and selection unit (16, 17), and a local power determination unit (18), wherein for a picture that is divided in a number of blocks (S_{11}-S_{58}), per block (S_{11}-S_{58}) the video levels or values derived from the video levels of the colour components of the pixels are summed up in order to determine the local power values (LP) for the picture, **characterised in that**, said apparatus further includes a local temperature estimator (19), that performs a local temperature estimation per block of the display based on

said local power values (LP) and the previously estimated local temperature values, a maximum local temperature selector (20) that selects the maximum local temperature from the estimated local temperatures, a maximum power level limit selector (21) that assigns a maximum power level limit to the selected maximum local temperature, and a power level limiter (22), wherein the power level limiter (22) restricts the range of selectable power level modes in the power level mode selector (21) to power level modes having a power level below or equal to said selected maximum power level limit (PLM).

8. Apparatus according to claim 7, wherein it is integrated in a plasma display device.

Claims

1. Method for power level control in a display device having a plurality of display elements corresponding to the pixels of a picture, wherein a power level mode selection process is used for increasing the peak white enhancement factor of the display, **characterised in that** a picture is divided in a number of blocks (S_{11}-S_{58}), wherein in each block (S_{11}-S_{58}) the video levels or values derived from the video levels of the colour components of the pixels are summed up in order to determine the local power values (LP) for the picture, wherein a local temperature estimation is performed based on said local power values (LP), wherein a step of determining the maximum local temperature (MT) in the display is performed, wherein a further step of maximum power level limit (PLM) determination is performed based on the determined maximum local temperature (MT), and wherein the power level limit (PLM) influences the power level mode selection process.

2. Method according to claim 1, wherein for local temperature estimation of a block (S_{11}-S_{58}), the power dissipation not only of the local block (S_{11}-S_{58}) but also of a number of neighbouring blocks (S_{11}-S_{58}) is taken into account.

3. Method according to claim 1 or 2, wherein the maximum local temperature determination for the display is performed once in a number of video frames.

4. Method according to claim 3, wherein the steps of local power value determination and local temperature estimation are performed for one or more selected blocks of the whole picture within a frame period only.

5. Method according to claim 3 or 4, wherein a picture is divided in 40 blocks and the maximum local temperature determination is performed once within 40 frame periods.

6. Method according to one of claims 1 to 5, wherein the switching between maximum allowed power level limits corresponding to the determined maximum local temperature is controlled with an hysteresis-like switching behaviour.

7. Apparatus for carrying out the method according to one of the previous claims, **characterised in that**, it includes a power level determination and selection unit (16, 17), a local power determination unit (18), a local temperature estimator (19), a maximum local temperature determination unit (20), a maximum power level limit selector (21) and a power level limiter (22) which influences the power level selection process for the display.

8. Apparatus according to claim 7, wherein it is integrated in a display device, in particular plasma display device.

Abstract

Method for power level control of a display device and apparatus for carrying out the method

Plasma Display Panels (PDP) are becoming more and more interesting for TV technology. One important criterion for picture quality is the Peak White Enhancement Factor PWEF. In a previous patent application a method for power level control in a display with which the PWEF can be increased has been proposed. With an increased PWEF the problem of local overheating of plasma cells may occur.
This invention proposes a protection circuit, which deals with this problem. For protecting the plasma display against local overheating, there is provided a method, which performs the steps of local power value determination (18), local temperature estimation (19), maximum local temperature determination (20) and maximum power level limit determination (21). The power level limit influences the power level control process (22) in the display device so that local overheating is avoided and the highest possible PWEF can be used. The invention also concerns a corresponding apparatus for carrying out the proposed method.

Fig. 5

Method for power level control of a display device and apparatus for carrying out the method

The invention relates to a method for power level control of a display device and an apparatus for carrying out the method.

More specifically the invention is closely related to a kind of video processing for improving the picture quality of pictures which are displayed on displays like plasma display panels (PDP), and all kind of displays based on the principle of duty cycle modulation (pulse width modulation) of light emission / reflection / transmission. Specific claim is laid on the aspect of panel temperature estimation for power level control.

Background

For image quality, peak white is of paramount importance. The Peak White Enhancement Factor (PWEF) can be defined as the ratio between the peak white luminance, to the luminance of a homogeneous white field, usually referred to as the full white level. CRT based displays have PWEFs of up to 5, first generation of PDPs were characterised by having a peak white to maximum average luminance ratio of about 2. This is far worse than what is achieved in old CRT technology.

A Plasma Display Panel (PDP) utilizes a matrix array of discharge cells, which could only be "ON" or "OFF". Also unlike a CRT or LCD in which grey levels are expressed by analogue control of the light emission, a PDP controls the grey level by modulating the number of light pulses per frame (sustain pulses). The eye will integrate this time-modulation over a period corresponding to the eye time response.

More sustain pulses correspond to higher peak luminance values. More sustain pulses correspond also to a higher power

that flows in the PDP. The PDP control can generate more or less sustain pulses as a function of average picture power, i.e., it switches between modes with different power levels. In this document, the Power Level of a given mode is defined as the number of sustain discharges activated for a region of 100 ire video. The available range of power level modes is regarded as approximately equal to the PWEF.

A previous European patent application of the applicant with application number 99101977.9 reports a technique that increases the PWEF of a PDP by increasing the number of available power level modes, in number and in range, and by introducing an hysteresis circuit in the luminance level selection control. This technique allows achieving PWEF values up to 5.

PDPs have a large surface. A PWEF of 5, although pleasant to the image quality, has the disadvantage that it may concentrate, under certain circumstances, for a long time, the power dissipation on a small surface of the panel. If this situation is prolonged for a long time, which may occur in case of still video, local overheating of the panel may assume unacceptable values.

It has been proposed in WO 99/30309 to provide a panel temperature detector beside an average picture level detector and a picture peak level detector in a PDP for the purpose of power level control.

Invention

The present invention has the object to further improve the power level control of displays, like PDPs. This object is achieved with the measures of claim 1. According to the invention a local temperature estimator is used instead of a simple temperature detector for power level control.

This has the advantage, that also in case of still pictures, in which only small areas have high luminance values, the panel can be reliably protected against local thermal overheating by switching over to lower power level modes.

This proposal can be used in combination with any peak white enhancement circuit providing a large PWEF factor, not only for PDPs.

In other words, one main idea behind this invention is to try to build a model that describes local overheating of a panel as a function of the displayed video picture, and to use that information to control the operation of the peak white enhancement loop.

The invention also concerns an advantageous apparatus for carrying out the method according to the invention. This apparatus contains practically speaking a thermal protection circuit for displays having a large PWEF, and comprises the following components:

1. A local power level determination unit.

2. A local temperature estimation unit.

3. A maximum local temperature determination unit.

4. A selector of the maximum allowed power level mode, as a function of the estimated maximum local temperature value. This function should include hysteresis, in order to prevent the occurrence of perceivable luminance oscillations.

5. A limiter of the current power level value, to the selected maximum allowed power level. This limiter actually performs the protection function because it determines the sub-field organisation and sustain pulse generation which

corresponds to the determination of the flow of energy into the PDP.

Advantageous additional embodiments to the claimed power level control method and apparatus are apparent from the dependent claims.

Drawings

Exemplary embodiments of the invention are illustrated in the drawings and are explained in more detail in the following description.

In the figures:

Fig. 1 shows an illustration for explaining the sub-field concept of a PDP;

Fig. 2 shows two different sub-field organisations to illustrate the concept of switching between different power level modes for peak white enhancement;

Fig. 3 shows a block diagram of a plasma display apparatus inclusive power level control apparatus such as known from EP 99101977.9;

Fig. 4 shows a hysteresis curve used for power level selection in the apparatus shown in Fig. 1;

Fig. 5 shows a block diagram of a plasma display apparatus inclusive power level control apparatus according to the invention;

Fig. 6 shows a first partition of the display panel into blocks of pixels for the local temperature estimation;

Fig. 7 shows a second partition of the display panel into blocks of pixels for the local temperature estimation with overlapping of blocks partly allowed;

Fig. 8 shows a third partition of the display panel into blocks of pixels for the local temperature estima-

tion with overlapping of blocks partly allowed and;

Fig. 9 shows a hysteresis curve used for maximum power level limit selection.

Exemplary Embodiments

The principles behind this invention are now explained by means of an example. It is strongly noted that values in an actual implementation may differ from those here shown, in particular the number and weight of the used sub-fields and the number of actual sustain pulses.

In the field of video processing is an 8-bit representation of a luminance level very common. In this case each video level will be represented by a combination of the following 8 bits:

$2^0 = 1$, $2^1 = 2$, $2^2 = 4$, $2^3 = 8$, $2^4 = 16$, $2^5 = 32$, $2^6 = 64$, $2^7 = 128$

To realise such a coding scheme with the PDP technology, the frame period will be divided in 8 sub-periods which are also very often referred to sub-fields, each one corresponding to one of the 8 bits. The duration of the light emission for the bit $2^1 = 2$ is the double of that for the bit $2^0 = 1$ etc. With a combination of these 8 sub-periods, we are able to build 256 different grey levels. E.g. the grey level 92 will thus have the corresponding digital code word %1011100. It should be appreciated, that in PDP technology the sub-fields consist each of a corresponding number of small pulses with equal amplitude and equal duration. Without motion, the eye of the observer will integrate over about a frame period all the sub-periods and will have the impression of the right grey level. The above-mentioned sub-field organisation is shown in Fig. 1. Note that Fig. 1 is simplified in that re-

spect that the time periods for addressing the plasma cells and for erasing the plasma cells after addressing (scanning) and sustaining are not explicitly shown. However, they are present for each sub-field in plasma display technology which is well known to the skilled man in this field. These time periods are mandatory and can be constant for each sub-field.

When all sub-fields are activated, the lighting phase has a relative duration of 255 relative time units. The value of 255 has been selected in order to be able to continue using the above-mentioned 8-bit representation of the luminance level or RGB data which is being used for PDPs. The second sub-field in Fig. 1 has e.g. a duration of 2 relative time units. In the field of PDP technology, the relative duration of a sub-field is often referred to the 'weight' of a sub-field, the expression will also be used hereinafter.

An efficient peak white enhancement control circuit requires a high number of discrete power level modes for mapping the 8 bit words of video signal level (RGB-, YUV-signals) to respective sub-field code words. Switching is done between the different power level modes as e.g. described in the European Patent Application 99101977.9 of the applicant. For the disclosure of the invention it is therefore also referred to the content of this application.

In Fig. 2 it is briefly shown how the principle of dynamic sub-field organisation works. Two modes with different power levels are shown.

In the first mode the sub-field organisation is composed of 11 sub-fields SF and in the second mode it is composed of 9 sub-fields. Each sub-field SF consists of an addressing period sc (scan period) where each plasma cell is charged or not charged determined by the code word for each pixel, a

sustain period su where the pre-charged plasma cells are activated for light emission and an erase period er, where the plasma cells are discharged. In the 9 sub-field case, less time is required for addressing (scan), and therefore more time is available for sustain pulses (the area in black is larger). The erase and scan time of a sub-field is independent of the corresponding sub-field weight. It can be seen from the figure, that the sub-field position and the sub-field weight is different for the two shown cases. For instance in the first shown case, the weight of the seventh sub-field is 32, and in the second case, the weight of the seventh sub-field is 64. The depicted relative time duration for addressing, erasing and sustain times are only exemplary and may be different in certain implementations. Also it's not mandatory, that the sub-fields with low weights are positioned at the beginning and the sub-fields with higher weights are positioned at the end of the field/frame period.

Supposed is a PDP device with a PWEF of 5. Video is coded from 0 to 255. Power level control generates a maximum of 5*255 sustain pulses (peak white) and a minimum of 255 pulses (full white), for 100 ire, in the mode with lower power level.

A solution was described using 4 different main modes:

Mode 1: 12 sub-fields (2*255 sustain pulses):
1 - 2 - 4 - 8 - 16 - 32 - 32 - 32 - 32 - 32 - 32 - 32

Mode 2: 11 sub-fields (3*255 sustain pulses):
1 - 2 - 4 - 8 - 16 - 32 - 32 - 40 - 40 - 40 - 40

Mode 3: 10 sub-fields (4*255 sustain pulses):
1 - 2 - 4 - 8 - 16 - 32 - 48 - 48 - 48 - 48

Mode 4: 9 sub-fields (5*255 sustain pulses):

1 - 2 - 4 - 8 - 16 - 32 - 64 - 64 - 64

Each of these 4 modes is subdivided in about 16 sub-modes, which use the same number of sub-fields, but which encode 100 ire to a different value (dynamic pre-scaling). A total of 67 sub-modes were listed, corresponding to 67 power levels (number of sustain pulses for 100 ire), increasing gradually from 255 to 1275.

The peak white enhancement circuit as disclosed in EP 99101977.9 is shown in Fig. 3.

RGB data is analysed in the average power measure block which gives the computed average power value (AP) for the whole picture to the PWEF control block. The PWEF control block, consults its internal power level mode table, taking into consideration the previous measured average power value and the stored hysteresis curve, and directly generates the selected mode control signals for the other processing blocks. It selects the pre-scaling factor (PS) and the sub-field coding parameters (CD) to be used. These are e.g. number of sub-fields, positioning of the sub-fields, sub-field weights and sub-field types. It also controls the writing of RGB pixel data in the frame memory (WR), the reading of RGB sub-field data from the second frame memory (RD), and the serial to parallel conversion circuit (SP) for addressing of lines. Finally it generates the SCAN and SUSTAIN pulses required to drive the PDP driver circuits.

Fig. 4, also already shown in patent application EP 99101977.9, shows a possibility for the dynamic control of the power level selection (pl) as a function of the measured picture average power (ap).

As it should be expected, when picture power level increases, modes are selected with decreasing power levels. There is an hysteresis loop in the control function. When picture average power is increasing, modes with power levels on the top line are chosen. When picture power is decreasing, modes with power levels on the bottom line are chosen. Points between the two lines can be chosen when the picture average power growth direction is modified. With this power level control method the power supply of a PDP is protected. An overload of the power supply in case of pictures with high average picture power values is avoided. On the other hand in case of low average picture power values more sustain pulses are produced and the power supply can provide the required current without being overloaded.

Fig. 5 depicts a peak white enhancement circuit with a thermal protection circuit for the PDP, which is the core of this invention. The blocks drawn in bold correspond to the blocks that constitute the protection circuit.

This protection circuit is based on a circuit described in another European patent application of the applicant with application number 99112906.5.

At first, the local power measurement block is described. The main idea is to divide the total display surface in many blocks S_{ij}, and then to integrate (add) the input video levels for all pixels in the block, which means for each pixel the video levels of the 3 colour components are added, thus obtaining a value P_{ij}:

$$P_{ij} = \Sigma(k \in S_{ij}) \ (R_k + G_k + B_k)$$

where k denotes all pixels belonging to S_{ij}.

Very bright small spots may be more objectionable with respect to thermal overheating than spots, having the same total power, but being somewhat larger. To handle this fact, it is suggested to square or even to cube the RGB pixel components, like in the following equations:

$$P_{ij} = \Sigma(k \in S_{ij}) \ (R_k^2 + G_k^2 + B_k^2)$$

$$P_{ij} = \Sigma(k \in S_{ij}) \ (R_k^3 + G_k^3 + B_k^3)$$

In Fig. 6, a first example of the partition of the plasma display surface in blocks S_{ij} is shown. For easiness of visualization, cells are presented with rounded edges, but in a practical implementation they will preferably be rectangular. In the shown example there is a total of 40 cells, but in an actual implementation the cell number might even be higher.

The partition of the total display surface in blocks S_{ij} can be improved, if overlapping of blocks is allowed, as e.g. shown in Fig. 7 and 8.

Without overlapping of blocks, if a bright spot occurs, for instance exactly at the border of 2 blocks, it might not be detected. With substantial overlapping of cells, there will always be a cell that comprises any bright spot, regardless of the bright spot position.

Next, the local temperature estimation in block 19 is explained. If the power being dissipated has been evaluated, the next step is to build a model that allocates to every picture block a local temperature value. It is pointed out that many models are possible, some very simple, some quite complex, and that a compromise in complexity will have to be found. Here, some of the possible approaches are mentioned, keeping in mind that even the simplest approximation is better than having no protection at all.

The temperature of a given block is, in a first approximation, equal to the previous temperature estimation $T(i,j)_{t-1}$, plus the power being dissipated $a \cdot P(i,j)_t$ in the block in the current frame period, minus a dissipation term D corresponding to the heat being given to the environment per frame time:

$$T(i,j)_t = T(i,j)_{t-1} + a \cdot P(i,j)_t - D$$

This model can be improved by making the assumption that the heat dissipation is proportional to the actual temperature:

$$T(i,j)_t = T(i,j)_{t-1} + a \cdot P(i,j)_t - b \cdot T(i,j)_{t-1}$$

Furthermore, thermal dispersion to the near-by blocks can also be considered:

$$T(i,j)_t = T(i,j)_{t-1} + a \cdot P(i,j)_t - b \cdot T(i,j)_{t-1} - c \cdot [\, T(i-1,j)_{t-1} - T(i,j)_{t-1} \,] - c \cdot [\, T(i+1,j)_{t-1} - T(i,j)_{t-1} \,] - c \cdot [\, T(i,j-1)_{t-1} - T(i,j)_{t-1} \,] - c \cdot [\, T(i,j+1)_{t-1} - T(i,j)_{t-1} \,]$$

The newly added terms can be either negative (if the near-by blocks are cooler) or positive (if the near-by blocks are hotter). Finally, for a last further refinement, diagonal thermal dispersion might also be considered by adding 4 further terms, but the complexity of the shown model should be enough for all practical purposes.

The above model also deals with the border effect. Blocks at the border, or at the corners will have less dissipation possibilities, due to the fact that they have less near-by blocks. They may overheat quicker, for the same power being

dissipated, but this should be correctly detected by the last here presented model.

Next, the maximum local temperature determination in block 20 is explained. In principle to find the maximum local temperature MT, it is required to evaluate, in the current example, the 40 P_{ij} values (40 = 5 rows * 8 columns) in block 18 and the corresponding 40 T_{ij} values in block 19, and then finding the maximum in block 20. This requires quite a number of operations per frame, with a large number of video integrators working in parallel.

Thermal heating is however a very slow process, and so the following approximation might be used:

1. For every frame the dissipation on a single picture block is calculated, i.e., power dissipation in every block is evaluated only once for every group of 40 frames (in this example).

2. For the selected picture block the local temperature is computed in block 19 using the following expression:

$$T(i,j)_t = T(i,j)_{t-40} + a\cdot P(i,j)_t - b\cdot T(i,j)_{t-40} - c\cdot[\, T(i-1,j)_{t-40} - T(i,j)_{t-40}\,] - c\cdot[\, T(i+1,j)_{t-40} - T(i,j)_{t-40}\,] - c\cdot[\, T(i,j-1)_{t-40} - T(i,j)_{t-40}\,] - c\cdot[\, T(i,j+1)_{t-40} - T(i,j)_{t-40}\,]$$

Here, the index t-40 means that the corresponding temperature value is an old value being calculated before, at maximum 40 frames before. Of course, the power dissipation term $a\cdot P(i,j)_t$ ignores all the power dissipations coming from the 40 frames between two temperature estimations for the same block and this is a drawback of the model. However it has been proofed that in practice this error is for TV pictures

acceptable. More expenditure for the temperature estimation can be reasonable for PDPs, which are used as a computer monitor where most pictures being displayed are still pictures.

3. Update the MT value (maximum temperature) in block 20. In order to do this it is required to know whether the block number $(i,j)_t$ for the MT value being determined, corresponds to the block $(i,j)max_{t-1}$ where the previous MT value (MT_{t-1}) was found.

If the block number is the same ($(i,j)_t = (i,j)max_{t-1}$):
Then $MT_t = T_{ij}$

If the block number is not the same ($(i,j)_t$? $(i,j)max_{t-1}$):
if ($T_{ij} > MT_{t-1}$)
then $MT_t = T_{ij}$
and $(i,j)max_t = (i,j)_t$
else
$MT_t = MT_{t-1}$

The above-mentioned algorithm is performed in block 20 of Fig. 5. This approximation reduces the evaluation complexity by a factor of 40.

Fig. 9 depicts the function of the maximum power level selection circuit 21. It shows the maximum allowed power level (plm) as a function of the estimated maximum panel local temperature (mt).

For low maximum local temperature values, no reductions in peak white level are required. For higher values, the maximum peak white level is gradually reduced. At the limit, in the figure, PWEF has been reduced from the original value of 5 to approximately 2 (full white corresponds to a power level of 255).

Some hysteresis, like the depicted hysteresis curve is built-in, in order to avoid small amplitude oscillations, mostly originating in errors of measurement, or in the displayed video noise.

The temperature estimation model is a model that reacts slowly to modifications in dissipated power. This is correct, because the panel temperature also reacts slowly to power being dissipated. Due to this slow reaction of the estimated panel temperature, it is sufficient for most applications, as explained above, that also the protection circuit reacts slowly, which has the additional advantage that its operation will not be perceived by the human viewer.

Last, the function of the power level limit block 22 will be explained. This circuit is a simple limiter that actuates only when dangerous local overheating has been detected. It does not change the function of the peak white enhancement circuit. It only limits the power level range available to the peak white enhancement control circuit. E.g., if the maximum power level value output from the block 21 is 765, then only the first 34 power level modes of EP 99101977.9 are selectable for PWEF control. The rest of the power level modes are forbidden.

The described circuit and algorithm performs a protection function, which means that, for most video pictures, it will have no effect, and only in case of a static bright spot, the peak white enhancement factor will be attenuated.

It can also be used for CRT based displays, where local overheating may cause local doming problems. Local doming, is a colour distortion of the picture, due to the local deformation of the CRT's mask, which is induced by local overheating of the tube colour mask.

It is also possible to have dynamic peak white control without having a protection circuit. Picture quality will however not be the same, because the dynamic peak white control will use a restricted range for the PWEF, in order to avoid unacceptable local thermal overheating.

Claims

1. Method for power level control in a display device having a plurality of display elements corresponding to the pixels of a picture, wherein a power level mode selection process is used for increasing the peak white enhancement factor of the display, **characterised in that** a picture is divided in a number of blocks (S_{11}-S_{58}), wherein in each block (S_{11}-S_{58}) the video levels or values derived from the video levels of the colour components of the pixels are summed up in order to determine the local power values (LP) for the picture, wherein a local temperature estimation is performed based on said local power values (LP), wherein a step of determining the maximum local temperature (MT) in the display is performed, wherein a further step of maximum power level limit (PLM) determination is performed based on the determined maximum local temperature (MT), and wherein the power level limit (PLM) influences the power level mode selection process.

2. Method according to claim 1, wherein for local temperature estimation of a block (S_{11}-S_{58}), the power dissipation not only of the local block (S_{11}-S_{58}) but also of a number of neighbouring blocks (S_{11}-S_{58}) is taken into account.

3. Method according to claim 1 or 2, wherein the maximum local temperature determination for the display is performed once in a number of video frames.

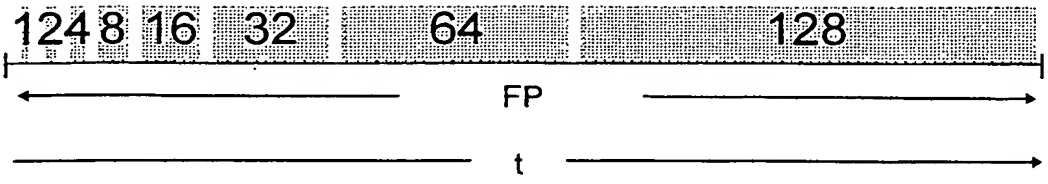
4. Method according to claim 3, wherein the steps of local power value determination and local temperature estimation are performed for one or more selected blocks of the whole picture within a frame period only.

5. Method according to claim 3 or 4, wherein a picture is divided in 40 blocks and the maximum local temperature determination is performed once within 40 frame periods.

6. Method according to one of claims 1 to 5, wherein the switching between maximum allowed power level limits corresponding to the determined maximum local temperature is controlled with an hysteresis-like switching behaviour.

7. Apparatus for carrying out the method according to one of the previous claims, **characterised in that**, it includes a power level determination and selection unit (16, 17), a local power determination unit (18), a local temperature estimator (19), a maximum local temperature determination unit (20), a maximum power level limit selector (21) and a power level limiter (22) which influences the power level selection process for the display.

8. Apparatus according to claim 7, wherein it is integrated in a display device, in particular plasma display device.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2
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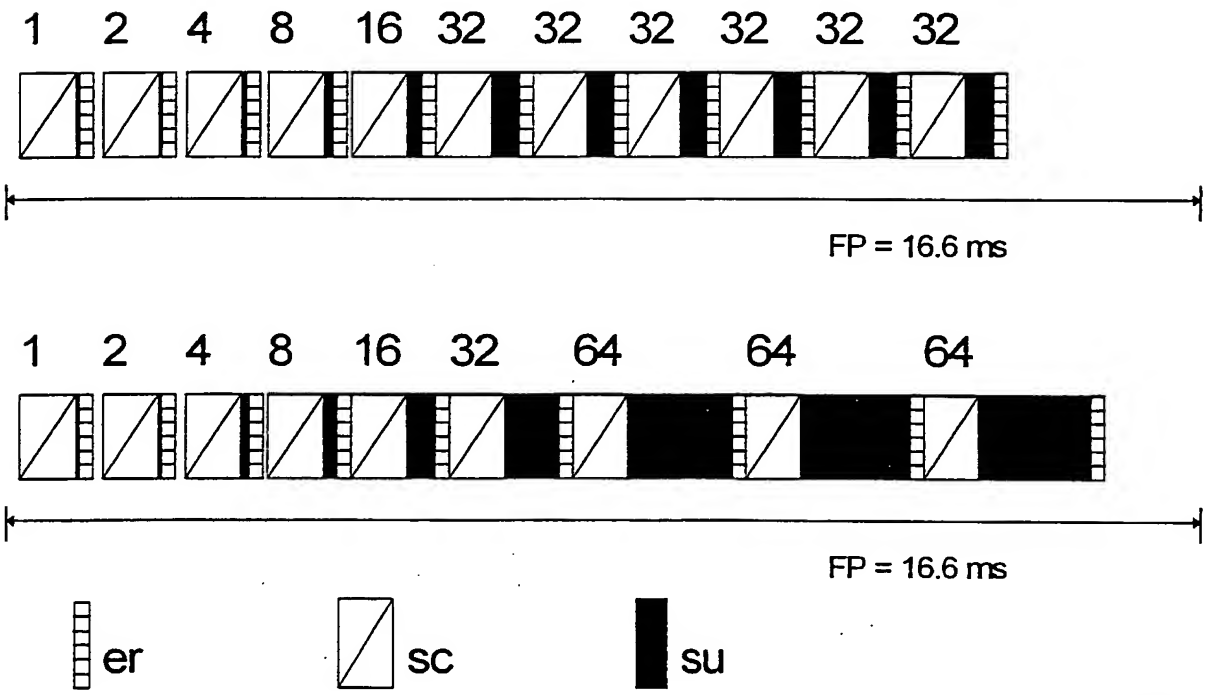
128
FP
t

Fig. 1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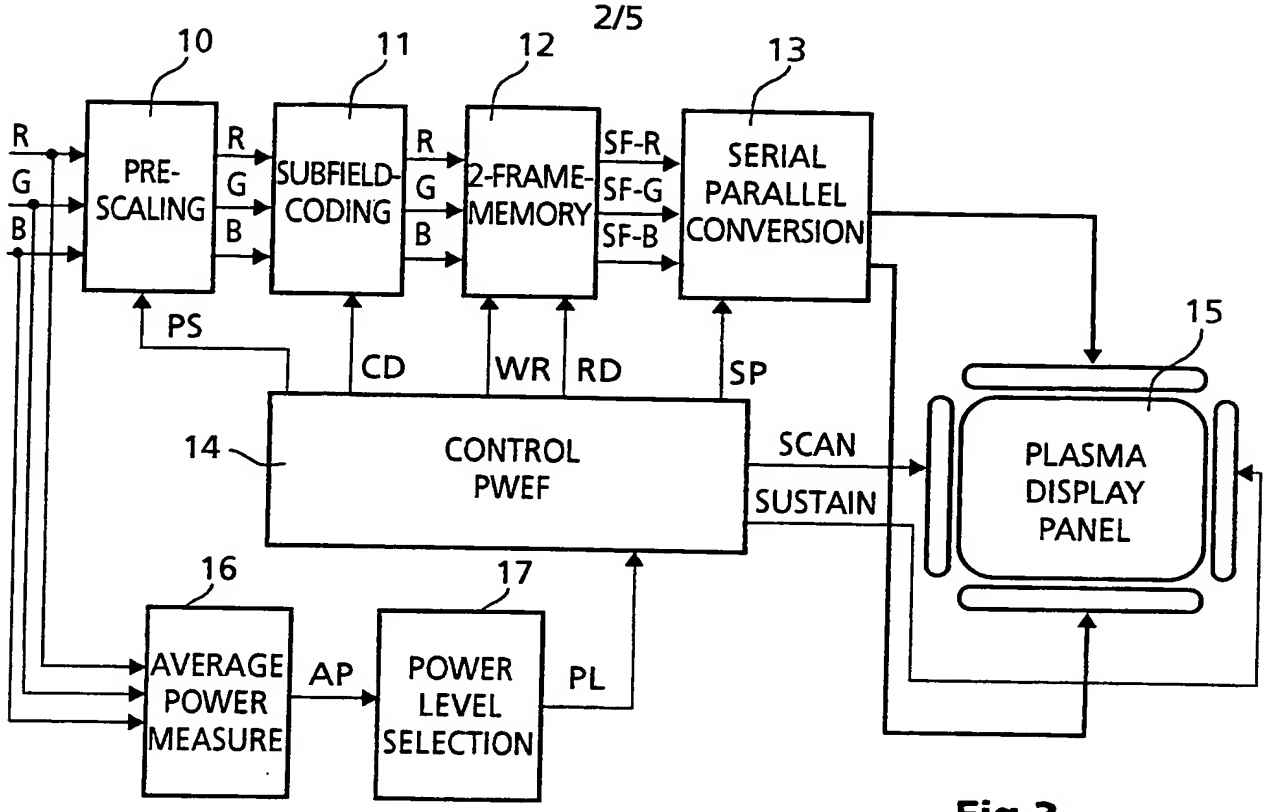
64
FP = 16.6 ms
er
sc
su

Fig. 2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G
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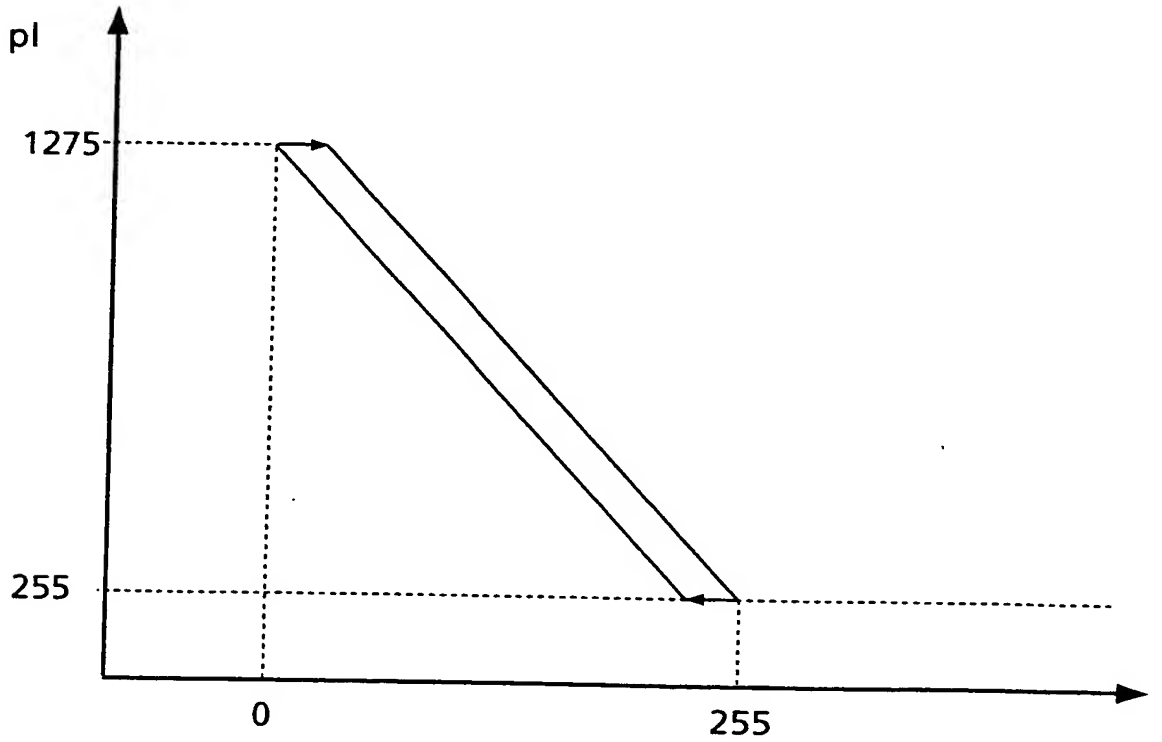
SERIAL PARALLEL CONVERSION
PS
CD
WR
RD
SP
15
14
CONTROL PWEF
SCAN
SUSTAIN
PLASMA DISPLAY PANEL
16
17
AVERAGE POWER MEASURE
AP
POWER LEVEL SELECTION
PL

Fig.3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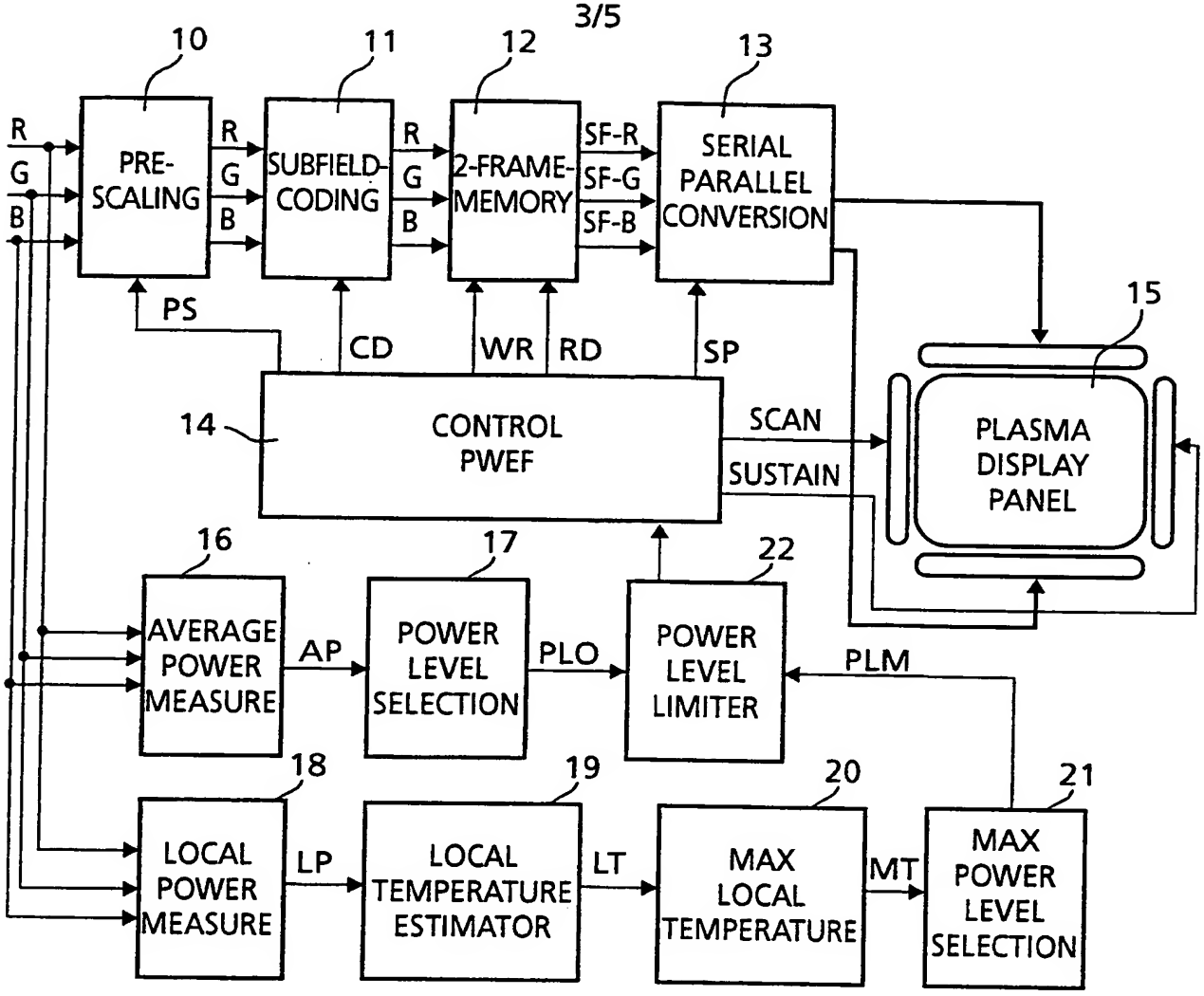
0
255
ap

Fig.4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CD
WR
RD
SP
15
14
CONTROL PWEF
SCAN
SUSTAIN
PLASMA DISPLAY PANEL
16
17
22
AVERAGE POWER MEASURE
AP
POWER LEVEL SELECTION
PLO
POWER LEVEL LIMITER
PLM
18
19
20
21
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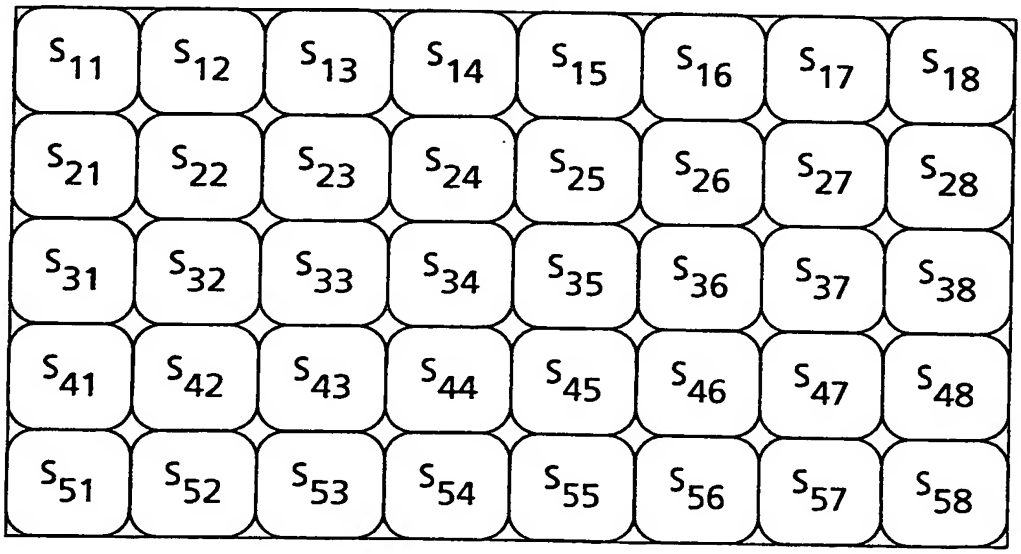
LP
LOCAL TEMPERATURE ESTIMATOR
LT
MAX LOCAL TEMPERATURE
MT
MAX POWER LEVEL SELECTION

Fig.5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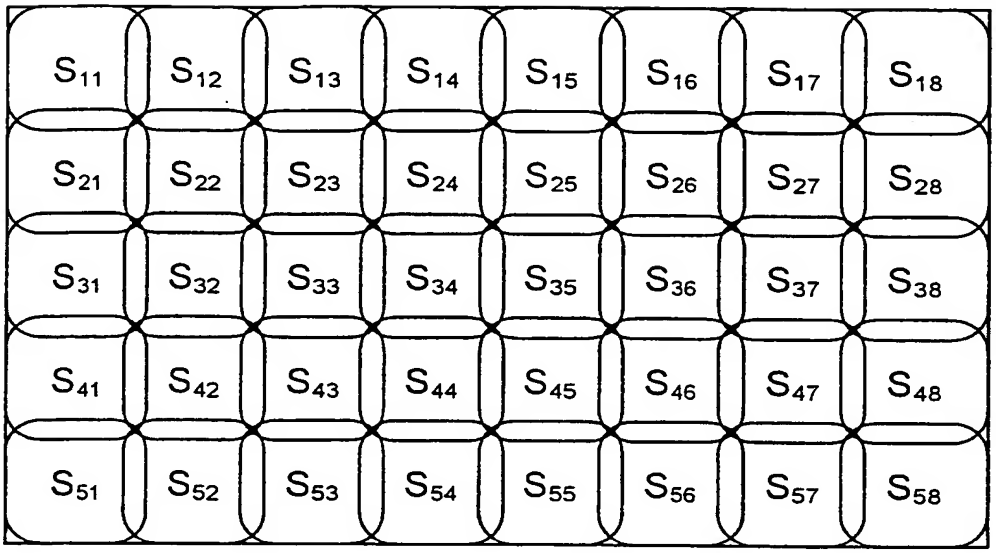
S21 S22 S23 S24 S25 S26 S27 S28
S31 S32 S33 S34 S35 S36 S37 S38
S41 S42 S43 S44 S45 S46 S47 S48
S51 S52 S53 S54 S55 S56 S57 S58

Fig.6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S21 S22 S23 S24 S25 S26 S27 S28
S31 S32 S33 S34 S35 S36 S37 S38
S41 S42 S43 S44 S45 S46 S47 S48
S51 S52 S53 S54 S55 S56 S57 S58

Fig. 7

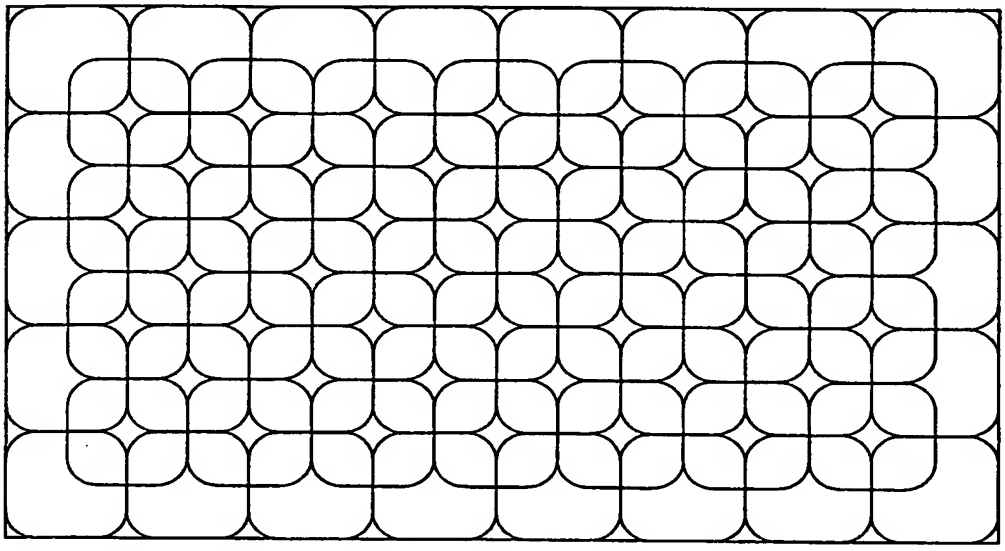

Fig. 8

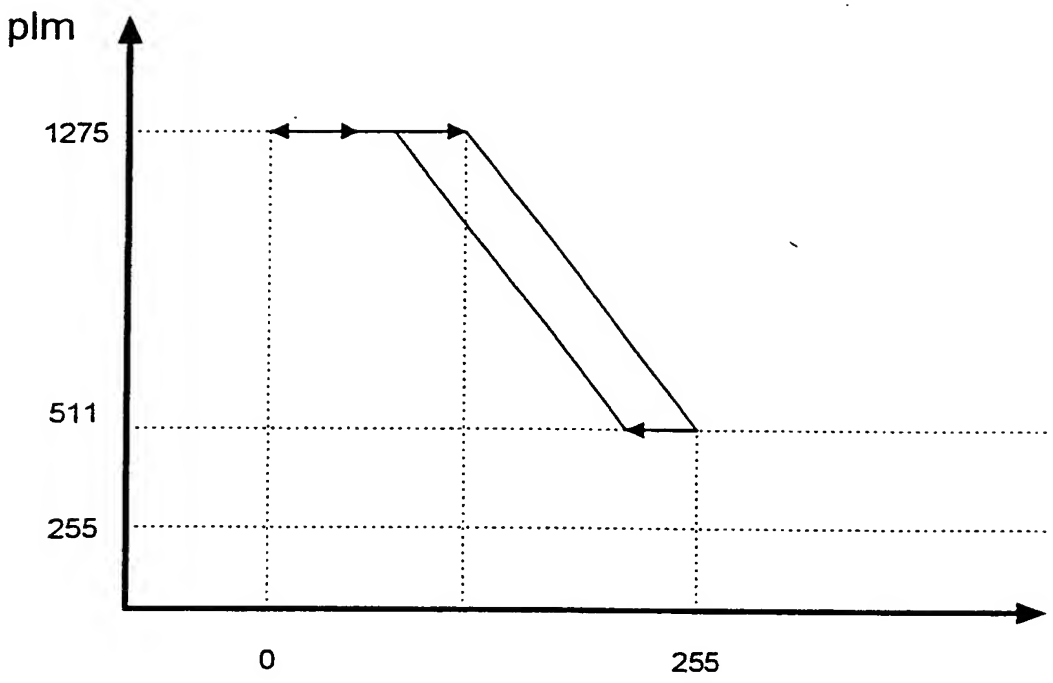

Fig. 9

INTERNATIONAL SEARCH REPORT

ional Application No
PCT/EP 00/07395

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G09G3/28

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 888 004 A (PIONEER ELECTRONIC CORP) 30 December 1998 (1998-12-30) abstract column 2, line 55 -column 3, line 45	1-4,7,8
A	column 10, line 58 -column 11, line 15; figures 1-6	5,6
A	EP 0 924 683 A (GRUNDIG) 23 June 1999 (1999-06-23) abstract column 1, line 3 - line 11 column 4, line 41 -column 5, line 25; figures 1-4	1-8

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
8 January 2001	24/01/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	O'Reilly, D

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/EP 00/07395

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 888004 A	30-12-1998	JP 11024631 A	29-01-1999
EP 924683 A	23-06-1999	DE 19756653 A	24-06-1999